Faculty of Electrical and Computer Engineering

Since 2012 the Technische Universität Dresden (TUD) is a part of the elected group of eleven Universities of Excellence in Germany. Furthermore, the Dresden location features the “Silicon Saxony”, which is the largest microelectronics cluster in Europe.

In the frame of the BMBF project MassiveData6G, the Chair of Circuit Design and Network Theory at the Institute of Circuits and Systems offers a position as

**Research Associate / PhD Student / Postdoc in Digital and Mixed-Signal Circuit Design**

(Subject to personal qualification employees are remunerated according to salary group E 13 TV-L)

The position is subject to financial commitment by the BMBF, starts on **1. June 2020** and is fixed termed until 30. September 2023. The period of employment is governed by the Fixed Term Research Contracts Act (Wissenschaftszeitvertragsgesetz - WissZeitVG). The position offers the chance to obtain further academic qualification (e.g. PhD or habilitation thesis).

The Chair of Circuit Design and Network Theory is a leading chair in the design of radio frequency, millimeter-wave and mixed-signal integrated circuits and has achieved several world records in these fields.

Within the scope of the project, an innovative transceiver architecture for future 6G applications with ultra-high peak data rates of 100 Gbit/s is being developed in close collaboration with our academic partners Technische Universität Berlin and Friedrich-Alexander Universität Erlangen as well as several industrial partners. The Chair of Circuit Design and Network Theory is responsible for the development, analysis, design and verification of the interface between the baseband processing architecture and the analog transmitter path RF frontend.

**Tasks:**
This vacancy of an "R&D digital and mixed-signal design engineer" offers you an excellent opportunity to develop yourself in a professional, team-oriented environment. As a member of our data converter design group you will be responsible for the conceptual planning, system architecture and block-level implementation of the digital components in a VLSI system. Your duties include the implementation and verification of digital blocks with experience in both back-end and front-end ASIC development flows, macro integration and implementation and design debugging. In particular, you will be consigned to develop RTL models, test benches and test cases and to execute the entire synthesis and physical implementation of digital IP including constraint development, static timing analysis and optimisation, place and route, DRC and LVS as well as functional verification by means of RTL and gate-level SDF-annotated mixed-signal simulations. Furthermore, you will oversee and assist our data converter designers in silicon debugging and documentation. You are required to publish scientific papers and attend project meetings and conferences.

**Requirements:**
We are looking for a candidate with very good or good university degree and if applicable a doctorate in electrical engineering, communications technology or information technology with profound knowledge in digital and mixed-signal circuit design. In particular, this includes strong Verilog/VHDL, Verilog-AMS, System Verilog and TCL scripting skills and a strong synthesis and STA background. Previous knowledge of the Universal Verification Methodology (UVM) and silicon debugging skills are beneficial. Interest in new technologies, an independent and flexible way of working, good communication and teamwork, excellent English (oral and written) and interpersonal skills as well as innovative and analytical thinking and high commitment are expected.
The job offer provides an excellent platform for interdisciplinary cooperation and the ability to push your personal scientific development in the course of a doctoral studies. Post doctorates have the opportunity to lead prestigious research projects. Applications from women are particularly welcome. The same applies to people with disabilities. Please submit your comprehensive application including copies of your CV and certificates until 12. March 2020 (stamped arrival date of the university central mail service applies) to **TU Dresden**, Fakultät Elektrotechnik und Informationstechnik, Institut für Grundlagen der Elektrotechnik und Elektronik, Professur für Schaltungstechnik und Netzwerktheorie, Herrn Prof. Ellinger, Helmholtzstr. 10, 01069 Dresden. Please submit copies only, as your application will not be returned to you. Expenses incurred in attending interviews cannot be reimbursed.

Reference to data protection: Your data protection rights, the purpose for which your data will be processed, as well as further information about data protection is available to you on the website: [https://tu-dresden.de/karriere/datenschutzhinweis](https://tu-dresden.de/karriere/datenschutzhinweis)