

TUD Dresden University of Technology, as a University of Excellence, is one of the leading and most dynamic research institutions in the country. For TUD diversity is an essential feature and a quality criterion of an excellent university. Accordingly, we welcome all applicants who would like to commit themselves, their achievements and productivity to the success of the whole institution.

At the **Faculty of Electrical and Computer Engineering, Institute of Circuits and Systems**, the **Chair of Highly-Parallel VLSI Systems and Neuro-Microelectronics** offers a position as

Research Associate / PhD Student / PostDoc (m/f/x)

(subject to personal qualification, employees are remunerated according to salary group E 13 TV-L)

starting **as soon as possible**. The position is limited until **May 31, 2029**. The period of employment is governed by the Fixed Term Research Contracts Act (Wissenschaftszeitvertragsgesetz - WissZeitVG). The position offers the chance to obtain further academic qualification (usually PhD / habilitation thesis). Balancing family and career is an important issue. The position is generally suitable for candidates seeking part-time employment. Please indicate the request in your application.

State-of-the-art AI systems depend heavily on models, providers and hardware from the U.S. and China, which represents a big challenge of Europe's sovereignty for AI model development and deployment (e.g., trustworthiness, dependability, performance, modularity). The Horizon Europe project OptimAIse (Optimising Performance and Trust for Integrity-driven Modular genAI Software Engineering) addresses these challenges by delivering a scalable, modular, and interoperable reference architecture that leverages European hardware to enable efficient and simplified large language model deployments. The SpiNNaker2 hardware, developed by TU Dresden and commercialized by SpiNNcloud, is one of Europe's most promising alternatives for the energy-efficient serving of LLMs. SpiNNaker2 is a massively parallel architecture with locally dense compute and globally sparse and low-latency communication, ideal to realize efficient AI models by leveraging sparse and event-based computing.

The candidate will develop and adopt LLMs for the SpiNNaker2 hardware. The models shall be implemented on the hardware using an existing software stack and optimized with ML compilers such as MLIR. Besides applying known approaches such as Mixture-of-Experts, the candidate shall follow the state of the art of efficient language models and try novel approaches on SpiNNaker2. In addition, the work will derive requirements and recommendation for next-generation AI hardware such as Spinnaker3, thus guiding the future of efficient AI systems.

Tasks:

- scientific research in efficient language models and their hardware deployment
- development and training of sparse and communication avoiding GenAI models optimized for SpiNNaker2 hardware
- implementation of GenAI models (resp. their layers) on SpiNNaker2 using ML compilers (e.g., MLIR)
- presentation and publication of research results in top-tier conferences/journals
- collaboration in European project OptimAIse, integrating GenAI models on SpiNNaker2 for use-case demonstrators

Requirements:

- university degree (Master's or equivalent) in computer science, electrical engineering, machine learning or related fields of expertise
- good understanding of LLMs and how they are processed on AI hardware for inference
- very good programming skills (e.g., C++, Python)
- good written and spoken English skills
- high motivation and ability to work independently and in teams
- excellent skills and practical experience in one or more of the following research areas is beneficial:
 - compiler frameworks (LLVM, MLIR)
 - embedded software development
 - computer and accelerator architectures
 - parallel and distributed computing

We offer:

- the opportunity to collaborate within a diverse team of multi-domain experts at HPSN chair
- access to the world's-largest brain-inspired supercomputer SpiNNcloud
- access to TUD's HPC environment for ML training
- flexible arrangements for work hours to support a good work-life balance
- 30 days of vacation per year (based on a 5-day workweek)
- extensive opportunities for professional development and continuing education
- health care and sports programs offered by TUD
- a discounted job ticket (also available as a Deutschlandticket)
- participation in the supplementary pension scheme for employees in the public sector via VBL (Federal and State Government Employees Retirement Fund)

TUD strives to employ more women in academia and research. We therefore expressly encourage women to apply. The university is a family-friendly university. We welcome applications from candidates with disabilities. If multiple candidates prove to be equally qualified, those with disabilities or with equivalent status pursuant to the German Social Code IX (SGB IX) will receive priority for employment.

Application: Please submit your detailed application with the usual documents (Cover letter, CV, degree certificate) quoting the **reference code HPSN_OptimAIse_2026** by **October 20, 2026** (stamped arrival date of the university central mail service or the time stamp on the email server of TUD applies), preferably via the TUD SecureMail Portal <https://securemail.tu-dresden.de> by sending it as a single pdf file to christian.mayr@tu-dresden.de or to:

TU Dresden, Chair of Highly-Parallel VLSI Systems and Neuro-Microelectronics, Prof. Christian Mayr, Helmholtzstr. 10, 01069 Dresden, Germany.

Please submit copies only, as your application will not be returned to you. Expenses incurred in attending interviews cannot be reimbursed.

TUD is a founding partner in the DRESDEN-concept alliance.

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Reference to data protection: Your data protection rights, the purpose for which your data will be processed, as well as further information about data protection is available to you on the website: <https://tu-dresden.de/karriere/datenschutzhinweis>.